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ESD-RELIABILITY INFLUENCES OF AN HV NLDMOS WITH DIFFERENT EMBEDDED SCR STRUCTURES IN THE DRAIN SIDE

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ABSTRACT

In this paper, implants of a P^+ continuous strip-type in the drain-end of nLDMOS to form nLDMOS-SCR embedded structures are investigated by a 0.25-µm 60-V BCD process. Here, the first part of this paper will aim to verify the influence of nLDMOS-SCR with different P^+ implant location on the anti-ESD ability. The I_{t2} value of a "pnp"-arranged type nLDMOS-SCR is 3 times more than that of an "npn"-arranged type nLDMOS-SCR. The second part is a dual embedded parasitic SCR structure, this architecture will result in the adjacent two fingers of MOSFETs don't have to share the same parasitic SCR. The results revealed a dual embedded parasitic SCR indeed has a higher I_{t2} value (up to 10.36% increasing) than that of a single embedded parasitic SCR.

KEYWORDS: Electrostatic Discharge (ESD), Embedded SCR, Holding Voltage (V_h), N-Channel Lateral Double-Diffused MOS (nlDMOS), Latch-Up Effect, Secondary Breakdown Current (I_{t2}), Trigger Voltage (V_{t1})

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Original Article

1. INTRODUCTION

High-voltage (HV) lateral double-diffused MOS (LDMOS) transistors are widely used in many areas nowadays, such as power electronics switching components, power management circuits, automotive electronics, and LCD driver [Nakamura et al. 2000; Wilson et al. 2003; Bagger et al. 2007; Ko et al. 2015]. However, an LDMOS has a very high operating voltage resulting in needing for better reliability and carrying large current ability, so effectively discharge large current has become very important.

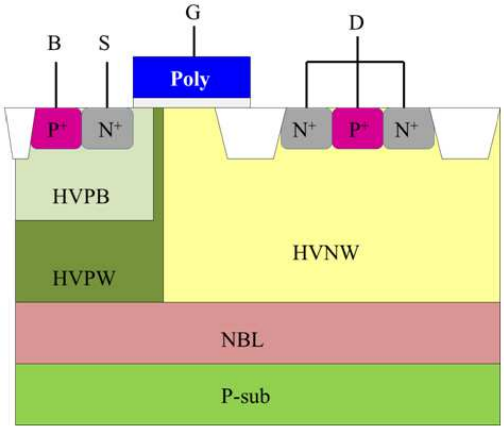
Meanwhile, the HV n-channel LDMOS (nLDMOS) is often self used to as an ESD protection element which is due to occupy fairly large layout, therefore need high efficient ESD protection elements in I/O pads [Lee et al. 2010; Cao et al. 2010; Wang et al. 2010; Chen et al. 2015]. It has several obviously disadvantages include V_{t1} too high, V_h too low and cannot uniform turn-on with multi-finger structure, result in low ESD level of per unit length for the HV nLDMOS. On the other hand, conventional SCRs [Huang et al. 2013; Lin et al. 2013; Wang et al. 2014] are used in low-voltage and high-voltage applications because they have a very strong ESD robustness. And, an HV SCR has a very strong ESD capacity of per unit length and is used in power circuit applications. But they still have some drawbacks, including higher V_{t1}, lower V_h etc. Recently, some studies combine these two devices [Pendharkar et al. 2000; Lee et al. 2002; Walker et al. 2007; Chen et al. 2015], using implanted a P^+ stripe on nLDMOS drain side to form an nLDMOS embedded with an HV SCR device (hereafter termed the nLDMOS-SCR). In these literatures, these are lacking in a systematic evaluation. Then, what will be really happened, and is there any other structure solutions for anti-ESD robustness? In this work, entire DUTs are fabricated by a 0.25-µm 60-V BCD process. The multi-finger structure of nLDMOS used in this work, the channel length (L) is kept to be 2-µm,

channel width of each finger (W_f) is 100-μm, finger numbers M= 6, and the total channel width (W_{tot}) is kept a constancy, 600-μm. The Reference (or benchmark) DUT was a pure nLDMOS.

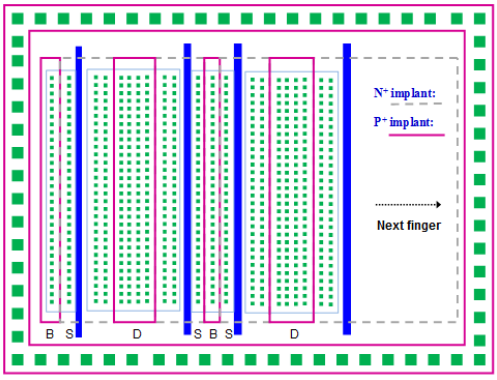
2. LAYOUT DESIGN OF HV DEVICES

2.1 HV nLDMOS with a Continuous Single-Embedded SCR in the Drain Side

Figures 1(a)~ 1(b) are the layout and cross-sectional view of HV nLDMOS-SCR, from that can be seen a parasitic SCR is formed by implanting P^+ in the middle of the drain side, we called this structure is the "*npn*"-arranged type nLDMOS-SCR in this paper (diffusion region of drain side is N^+-P^+-N^+). Then, changing the implant locations of P^+ implants in both side of N^+ region as shown in Figures 2(a)~ 2(b). We called this structure is the "*pnp*"-arranged type nLDMOS-SCR in this paper. By using these two different layouts to verify only changing the implant location of P^+ will create what kind of changing to the anti-ESD immunity. In order to enhance the accuracy of results, all of the layout size in the drain side, the area ratio of P^+ and N^+, and the total contact numbers are fixed. Thus, only the implant position of P^+ is varied.

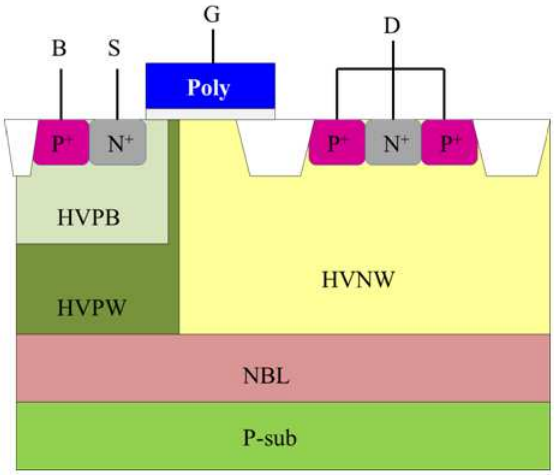


(a)

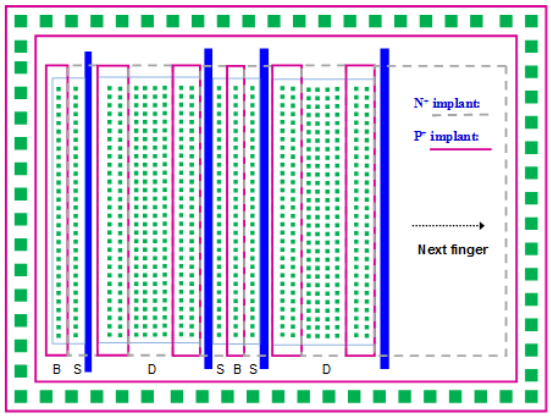


(b)

Figure 1: (a) Cross-Sectional View; and (b) Layout Schematic Diagram of the HV nLDMOS with a Continuous Stripe "*npn*"-Arranged Type in the Drain-Side



(a)

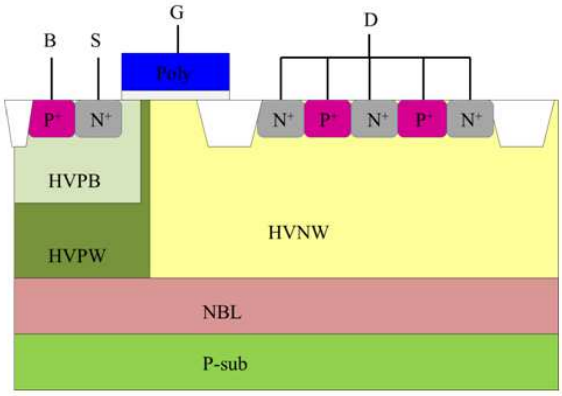


(b)

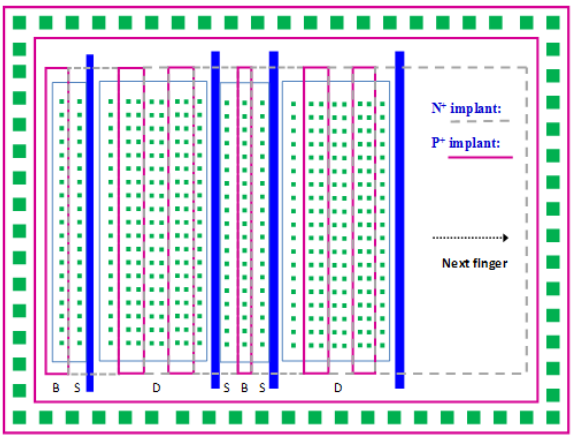
Figure 2: (a) Cross-Sectional View; And (b) Layout Schematic Diagram of the HV nLDMOS with a Continuous Stripe "*pnp*"-Arranged Type in the Drain-Side

2.2 HV nLDMOS with Continuous Dual-Embedded SCRs in the Drain Side

We extend the concept of section 2.1, because one embedded SCR structure is adjacent two stripe MOSTs and shared the same parasitic SCR ability in the previous section. Therefore, we bring an idea let one parasitic SCR split into two parasitic SCR in the drain side, two split P^+ diffusion region will be implanted in the drain side, let each finger of MOST has a reserved parasitic SCR ability. Therefore, the drain side will be divided into five regions; the drain side will be formed as an nLDMOS-SCR with the "*npnpn*"-arranged type or the "*pnpnp*"-arranged type. These new structures are shown in Figures 3~ 4. In the same time, all of the layout size in the drain side, the area ratio of P^+ and N^+, and the total contact numbers are kept same as the previous DUTs (shown in Figures 1~2). Thus, only the implant location of P^+ is altered. The anti-ESD capability of dual embedded SCRs will be verified and compared with a traditional nLDMOS (none with any parasitic SCR structure), which is taken as the standard reference DUT.

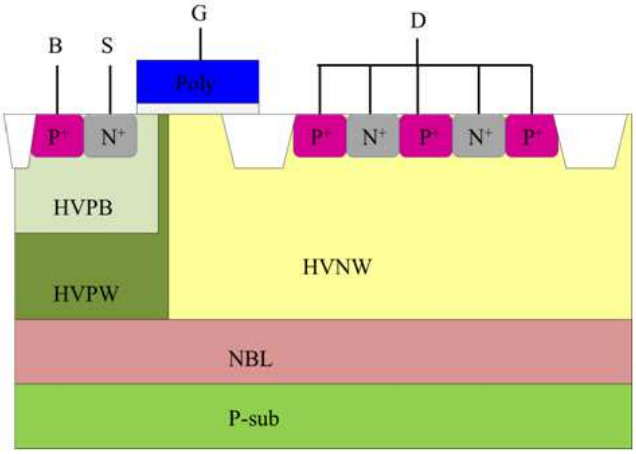


(a)

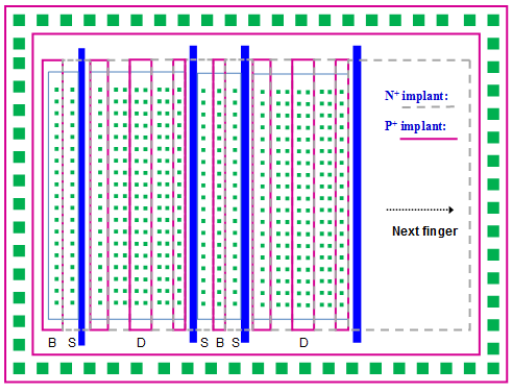


(b)

Figure 3: (a) Cross-Sectional View; And (b) Layout Schematic Diagram of the HV nLDMOS with Continuous Stripe "*npnpn*"-Arranged Type in the Drain-Side



(a)



(b)

Figure 4: (a) Cross-Sectional View; and (b) Layout Schematic Diagram of the HV nLDMOS with Continuous Stripe "*pnpnp*"-Arranged Type in the Drain-Side

3. TLP TESTING EQUIPMENT SYSTEM

A transmission-line-pulse (TLP) system for experimental testing is controlled by the LabVIEW software. It managed the subsystem electrical machine such as the ESD pulse generator, the high-frequency digital oscilloscope and the digital power electric meter instruments to achieve the automatic measurement. This machine can provide a continuous step-high square wave to device, and short raise time of the continuous square wave can also simulate transient noise of ESD. This HBM-like system has used the short square wave with 100ns pulse widths and 10ns rising/falling times to evaluate the voltage and current response of device. These short pulses in a TLP are used to simulate an ESD wave acting on a protective device. Therefore, the I-V characteristics of device can be obtained, such as the trigger voltage (V_{t1}), trigger current (I_{t1}), the holding voltage (V_h) and holding current (I_h), the secondary breakdown voltage (V_{t2}) and current (I_{t2}).

4. MEASURE RESULTS AND DISCUSSIONS

Each layout-type of nLDMOS-SCR DUTs with continuous stripe distributions in the drain-side had been tested, the TLP data shown in Figure5 and Table 1. From these data, we can see that the I_{t2} values of the "*pnp*"-arranged type and "*pnpnp*"-arranged type are much larger than that of the "*npn*"-arranged type and "*npnpn*"-arranged type among these nLDMOS-SCR DUTs (more than 2.91 ×) whatever types. Due to the electric power limitation of this TLP measurement system, a measurement will be stopped when the internal current of DUTs is more than 9 A. The N^+ diffusion region of "*pnp*"-arranged type and "*pnpnp*"-arranged type among an nLDMOS-SCR in the drain-side is far away from the shallow-trench-isolation (STI) region, the high field (or hot spot) which generated by N^+/HVNW junction far away from the STI region, too. In the same time, the major ESD dissipation region, i.e. an embedded SCR, is implemented in a shorter path. These distinguishing features make the ESD robustness of "*pnp*"-arranged type and "*pnpnp*"-arranged type higher than that of "*npn*"-arranged type and "*npnpn*"-arranged type among these nLDMOS-SCR DUTs.

And, the event which is worth paying attention, the anti-ESD abilities of the "*npn*"-arranged type and "*npnpn*"-arranged type are worse than the Ref. DUT (pure nLDMOS). The I_{t2} values decreased for the parasitic embedded "*npn*"-arranged type SCRs (13.31% decreased) and the parasitic embedded "*npnpn*"-arranged type SCRs (4.33% decreased) as compared with the Ref. DUT. Therefore, the ESD robustness can't be efficiently increased with these embedded SCRs. Nevertheless, the I_{t2} value of "*npnpn*"-arranged type is higher than that of the "*npn*"-arranged type (10.36% increased); this means that a complete parasitic SCR structure which can be used is good for anti-ESD capability.

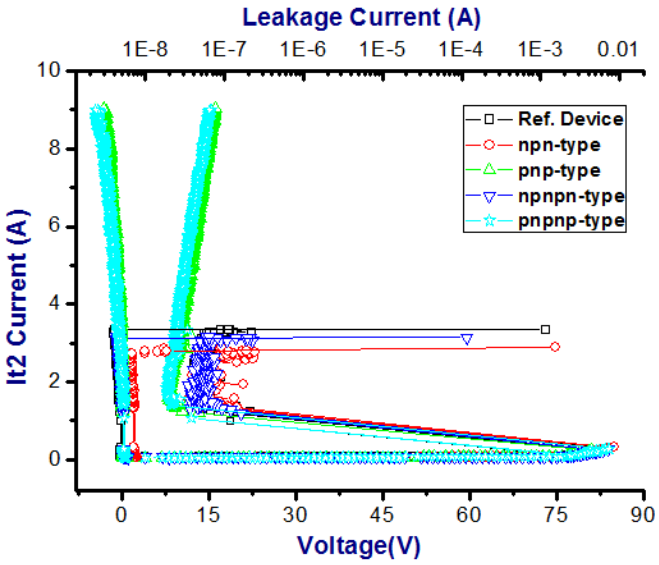


Figure 5: High-Current Snapback Curves and Leakage Currents of Nldmos Duts with Various Drains Engineering (Continuous Stripe Scrs)

Table 1: High-Current Snapback Parameters of an nLDMOS with various Drains Engineering (σ Was Calculated by 3 Samples)

nLDMOS_SCR (W_f=100μm)		V_{t1} (V)	V_h (V)	I_{t2} (A) (mean ± σ)
Continuous Stripe Type	Ref. Device	84.96	13.5	3.23 ± 0.17
	npn-type	84.42	13.47	2.8 ± 0.21
	pnp-type	81.03	9.3	>9
	npnpn-type	84.70	12.92	3.09 ± 0.11
	pnpnp-type	84.70	8.57	>9

5. CONCLUSIONS

From this paper, it can be found that the P^+ implanted location of an nLDMOS with embedded SCRs in the drain-side will have a strong impact on the anti-ESD robustness. In continuous stripe styles, the "*pnp*"-arranged type has a better I_{t2} value as compared with the Ref. DUT and "*npn*"-arranged type, the I_{t2} value of "*pnp*"-arranged type are 3 times than that of an "*npn*"-arranged type. Similarly, as for the continuous dual embedded SCRs, the "*pnpnp*"-arranged type has better I_{t2} values (which greater than that of the "*npnpn*"-type about 3 times); and the "*npnpn*"-arranged type have a better I_{t2} value as compared with the "*npn*"-arranged type. Therefore, it confirms that a complete parasitic SCR which shared by one nLDMOS has higher ESD robustness than that it shared with two adjacent devices.

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